REMARKS

Claims 23-31 were pending in the above referenced application, Claims 32-35 are added. The subject matter of such new claims is fully supported in the specification, for example at page 8, thus such new claims do not add new matter. It follows then that Claims 23-35 are currently pending..

The title is amended in accordance with the Examiner's suggestion and the Abstract is amended to be reflective of the subject matter of this Divisional Application.

Applicant submits herewith, a copy of the Supplemental Information Disclosure Statement with PTO form 1449 that was filed with the Office, December 20, 2001. Citation of these references is respectfully requested in the Examiner's next action. In addition, Applicant requests that the Examiner indicate in the next action whether or not the drawings for this application, submitted April 26, 2000, have been approved, for example by appropriately marking Item # 10 on the Office Action Summary.

Rejection under 35 U.S.C. §102

Claims 23-25, 27 29-31 stand rejected under 35 U.S.C. §102(e) as being anticipated by US 6,133,613 to Yao et al. (hereinafter "Yao"). Applicant traverses.

Applicant provides, herewith, a Declaration under 37 C.F.R. §1.131. Such declaration by the first named inventor of the instant application, Zhiping Yin, establishes that the subject matter claimed was conceived and actually reduced to practice prior to the 102(e) date of Yao. Therefore, Yao is not prior art and the rejection under §102(e) must be withdrawn. Action to this effect is requested.

Rejections under 35 U.S.C. §103

Claims 26 and 28 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yao in view of US 5,833,011 to Lin et al. (submitted by applicant) (hereinafter "Lin"). Applicant traverses.

B

As a result of the above referenced Declaration, the primary reference cited by the Examiner is not prior art and thus not available for use in a rejection under §103. As the Examiner does not allege and as Lin does not in fact teach or suggest all aspects of Claims 26 and 28, in the absence of Yao, the instant rejection must be withdrawn, which action is earnestly sought.

In summary, Applicant having responded to each of the rejections and objections, respectfully asserts that Claims 23-31 are in condition for allowance. In addition, Applicant asserts that new Claims 32-35, depending from Claims 23 and 27, respectively, are also in condition for allowance. Action to that effect is earnestly sought. If, however the Examiner's next action is anything other than a Notice of Allowance, the Examiner is requested to call the undersigned to schedule a telephonic interview. The undersigned is available during normal business hours, Pacific Coast Time.

Respectfully submitted,

Dated: Jan 22, 2002

By: _____
Bernard Berman
Reg. No. 37,279

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/559,903
Filing Date ..... April 26, 2000
Inventor ..... Ardavan Niroomand et al.
Assignee ..... Micron Technology, Inc.
Group Art Unit 2815
Examiner ..... G. Eckert II
Attorney's Docket No. MI22-1427
Title: Circuitry and Gate Stacks Encompassing a Semiconductive Substrate, A Metal Silicide Layer And An Inorganic Material Layer In Physical Contact With The Metal Silicide Layer (as amended)

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO OCTOBER 3, 2001 OFFICE ACTION

None of Claims 23-31 are amended.

Claims 32-35 are added.

The Abstract has been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

B

~~In one aspect, the~~ The present invention includes ~~a~~ semiconductor ~~processing method comprising a)~~ circuitry. Such circuitry encompasses ~~forming~~ a metal silicide layer over a substrate~~; b) depositing~~ and a layer comprising silicon, nitrogen and oxygen ~~over~~ in physical contact with the metal silicide layer~~; and c) while the layer comprising silicon, nitrogen and oxygen is over the metal silicide layer, annealing the metal silicide layer~~. ~~In another aspect, the~~ The present invention also includes a gate stack ~~forming method, comprising a)~~ which encompasses ~~forming~~ a polysilicon layer over a substrate~~,~~; ~~b) forming~~ a metal silicide layer over the polysilicon layer~~,~~; ~~c) depositing~~ an antireflective material layer over the metal silicide layer~~,~~; ~~d) forming~~ a silicon nitride layer over the antireflective material layer~~,~~; ~~e) forming~~ and a layer of photoresist over the silicon nitride layer~~,~~; ~~f)~~ for photolithographically patterning the layer of photoresist to form a patterned masking layer from the layer of photoresist~~;~~ and ~~g)~~ transferring a pattern from the patterned masking layer to the silicon nitride layer, antireflective material layer, metal silicide layer and polysilicon layer. ~~to pattern the~~ The patterned silicon nitride layer, antireflective material layer, metal silicide layer and polysilicon layer encompass ~~into~~ a gate stack. ~~In yet other aspects, the invention encompasses circuitry and gate stacks.~~

B

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

EV026160375US

Application Serial No.	09/559,903
Filing Date	April 26, 2000
Inventor	Zhiping Yin et al.
Assignee	Micron Technology, Inc.
Group Art Unit	2815
Examiner	G. Eckert II
Attorney's Docket No.	MI22-1427

Title: Circuitry and Gate Stacks

DECLARATION UNDER 37 C.F.R. §1.131

I, Zhiping Yin, do declare the following.

(1) That I am the first named inventor on the above-identified patent application which is assigned to Micron Technology, Inc.

(2) That I am currently employed as a Senior Engineer by Micron Technology, Inc., in Boise, Idaho, my employment with Micron beginning in December, 1996.

(3) That I graduated from Lanzhou University with a Bachelor of Science degree in Physics in 1981.

(4) That I received a Doctorate (Ph.D.) degree from City College of New York (CCNY) in Physics in 1991.

(5) That I am a named inventor on 12 issued patents.

(6) That the subject matter of the above-identified patent application was conceived on or before February 12, 1997 as indicated in **¶3.3.1.a** of the attached copy of the signed and dated "Invention Disclosure" (Attachment 'A').

(7) That the subject matter of the above-identified patent application was actually reduced to practice on or before July 8, 1997 as indicated by the "Surface Analysis Report" dated March 22, 1997 (Attachment 'B') and the "Inorganic ARC Fab 4 Process Development" meeting dated July 8, 1997 (Attachment 'C'). Specifically these meeting notes show:

a) Surface Analysis Report: that a DARC film was prepared for analysis on or before the date of the report. That the DARC film composition is shown by XPS analysis to comprise, at least, silicon, oxygen,

and nitrogen and silicon is bonded as silicon nitride and silicon oxide as well as a third component. That further FTIR analysis identified the third component as being Si-H.

b) Inorganic ARC Fab 4 Process Development meeting notes: that on page 2 of the notes, the section headed D72A-50, indicates that the split lots were used to optimize a nitride capping layer thickness overlying the DARC film. The table of this section showing the use of films identified as DARC320, where the 320 designates the film thickness as indicated as well as a indication of a specific DARC recipe, with nitride cap layers of both 1780 Angstroms and 1900 Angstroms. that on page 3 of notes, the a PROLITH/2 simulation report summary indicates that a stack composition comprising (1) a silicon substrate overlaid with (2) a tungsten silicide layer which is overlaid with (3) a DARC layer which is overlaid with (4) a silicon nitride layer, the stack being finally overlaid with (5) a photoresist layer.

(8) That when taken as a whole, the Invention Disclosure, the Surface Analysis Report and the Inorganic ARC Fab 4 Process Development meeting notes demonstrate that the subject matter of the above identified patent application was conceived and reduced to practice on or before July 8, 1997.

(9) That all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of United States Code, and may jeopardize the validity of the application or any patent issuing thereon.

Date: 1/22/2002 By: Zhiping Yin

If ARPA project, please check below:

___ Advanced SRAM
___ BST
___ FED
___ FIE RAM
___ NCAICM

INVENTION DISCLOSURE

97-857

1. INVENTOR(S): Zhiping Yin, Ravi Iyer, Tom R. Glass, Rick Holscher, Ardavan Niroomand, Linda Sommerville, Gurtej Sandhu

2. DESCRIPTION

2.1 Title of invention:

Using DARC films as anti-reflective coating and oxide cap in a process.

2.2 Brief description:

Dielectric anti-reflective coating (DARC) film has been applied at 50 level to improve the photo performance for I-line and DUV lithography and also to replace the 350A low silane oxide on the top of Wsix acting as a oxide cap to prevent the fuzz balls during the Wsix anneal. Since Wsix anneal in the 50 level process affects the DARC film thickness, n, and k value, the thickness, n, and k values are optimized to post-anneal values to give the lowest reflectivity from the 50 stack.

2.3 Also attach a complete description, including drawings or sketches and articles relevant to the invention. Legible photocopies of laboratory notebooks are acceptable.

See attach Fig.1

3. INFORMATION CONCERNING CONCEPTION OF INVENTION

3.1 CONCEPTION AND DOCUMENTATION OF THE INVENTION

a. Identify the date when you first conceived the invention. (If not sure, give the earliest date of which you are sure.)

Feb. 12, 1997.

b. To whom was the idea first described and on what date? (Other than a co-inventor.)

c. Identify the date of the first tangible record such as computer simulation, tape out, drawing or written description. Please specify type and location.

ATTACHMENT 'A'

3.2 CONCEPTION OF THE INVENTION

a. Please identify related invention disclosures, patents or other publications describing similar ideas, and other companies working in the same field. Attach copies, if available.

b. What is the closest technology, of which you are aware?

BARC technology.

c. Identify the advantages of this invention over previous technology.

DARC film is an inorganic film which will eliminate the contamination given by the organic BARC film for photo performance. In addition, the DARC film is Si-rich oxide film. It can replace the 350 A low silane oxide film in 50 stack process acting as oxide cap. Therefore, the application of one DARC film in 50 level will give both function as oxide cap and BARC at previous 50 stack. It is a more clean process than the previous process. In addition, it will save the process time and the cost by using cheap DARC replace BARC.

3.3 IMPORTANT DATES

a. Has the invention been disclosed outside the company? _No.____ If yes, to whom, when, and in what form?

b. Have any articles describing your invention been published? _____ If yes, list author(s), title of article, publication and date.

c. Have any engineering samples been given out? _____ If yes, to whom and on what date?

d. Has any product using the invention been sold or offered for sale? _____ If yes, to whom and on what date?

3.4 DISPOSITION OF THE INVENTION

a. When will (or did) Micron begin use of the invention experimentally?

b. When will (or did) Micron begin production of this invention?

3.5 MISCELLANEOUS I...ORMATION

a. Was the invention developed during a joint development agreement or other contract with an outside company? _____

b. Please list developmental work outside of the company (including Government proposal or contract).

INVENTORS:

ame: Zhiping Yin

icron Phone: 84032_____ Micron Mail Stop: __306_____

ompany Name(VERY IMPORTANT): Dept. Name: _____
___ Micron Technology, Inc. Dept. #: _____
___ Micron Electronics, Inc.
___ Micron Quantum Devices
___ Micron Display Technology, Inc.
___ Micron Communications, Inc.
___ Other_____

ome Address: _113 E Mallard Dr. #282_____

Boise, ID 83706 _____

itizenship: P. R. C.

upervisor: _Gurtej Sandhu_____

ignature: Zhiping Yin Date: 7/17/97

ame: _Ravi Iyer_____

licron Phone: _____ Micron Mail Stop: _____

ompany Name(VERY IMPORTANT): Dept. Name: _____
___ Micron Technology, Inc. Dept. #: _____
___ Micron Electronics, Inc.
___ Micron Quantum Devices
___ Micron Display Technology, Inc.
___ Micron Communications, Inc.
___ Other_____

ome Address: _____

_____

itizenship: _____

upervisor: _____

ignature: Ravi Iyer Date: 7/17/97

SURFACE ANALYSIS REPORT

Date: 22 March 1997

To: D. Yates, W. Lee, and A. Yin

From: C. A. Bradbury

Re: Job # 970307005-XPS ANALYSIS OF DARC OXIDE ON SILICON

Ref: Data table file 70307005.xls

Results and Discussion:

A wafer with DARC oxide on monocrystalline silicon was submitted for XPS analysis. A profile of the sample was included below. The elements detected in the layer were silicon, nitrogen, and oxygen. The silicon peak (figure 2) had three species present a nitride, an oxide, and a third peak with energy slightly higher than elemental silicon. This third peak was thought to be Si-H. The sample was then analyzed using FTIR which can show bonding between silicon and hydrogen. The resulting spectra had peaks indicative of Si-H.

The referenced data table contains the atomic concentrations for all elements detected and the individual silicon species.

If you have any questions regarding this information, please call 8-3589, 8-5944 or 8-1275.

Cynthia

ATTACHMENT 'B'

[redacted]

Inorganic ARC
Fab 4 Process Development
July 8,1997

Film Deposition Update

[redacted]

I-line Update

- [redacted]
- [redacted]

[redacted]

DUV Update

- [redacted]

[redacted]

-SWR 25772 on M9-45277.1 through probe. Wafer #23 yielded 649DPW!

-All lots currently running on the DARC320 Recipe.

[redacted]

- [redacted]

[redacted]

ATTACHMENT 'C'

- [redacted]

- D72A-50

  -DARC320 to be tested on upcoming Topography lot. Lot will be split 50/50 between the current 1900A nitride cap and the simulated optimum cap of 1780A. CD Swing Curve and CD variation across the wafer to be done. Proposed Splits (CDENNISON) on 2 short loop topo lots

DARC	Nitride
DARC320 (320A)	1780A
DARC320 (320A)	1900A (Current)
DUV DARC (500A)	1780A

- [redacted]

Parameter File: default.par
Speed Factor: 5

PROLITH/2

The Positive/Negative Resist Optical Lithography Model, v5.07

5 Jun 1997

Resist: Positive Thickness = 950.0 nm
Layer # 1: Si Nitride Thickness = 300.0 nm
Layer # 2: DARC anealed□□;M Thickness = 32.0 nm
Layer # 3: Wsix, annealed Thickness = 125.0 nm
Substrate: Silicon